Faculty of Electrical Engineering / ELECTRONICS, TELECOMMUNICATIONS AND COMPUTERS / VLSI DESIGN

Course:	VLSI DESIGN			
Course ID	**Course status**	**Semester**	**ECTS credits**	**Lessons** (Lessons+Exercises+Laboratory)
5164	Mandatory	1	6	3+1+0
Programs	ELECTRONICS, TELECOMMUNICATIONS AND COMPUTERS			
Prerequisites	There are no conditions for registration and course attending.			
Aims	Students are met with the basics of very large scale integration circuit design: basic active electronic components, CMOS inverter, bilateral CMOS switch, planar process, estimation of R, C, and L parameters, dynamic characterization of circuits, digital integrated circuits, analog integrated circuits.			
Learning outcomes	Once a student passes the exam, he will be able: 1. To give and to explain: the types of substrates, fabrication technologies, fabrication techniques, integration scales, and semiconductor integrated circuit design methodologies. 2. To perform a detailed analysis of CMOS inverter and bilateral CMOS switch. 3. To perform an estimation of resistances, capacitances and inductances of active and passive components in semiconductor integrated technologies. 4. To model and analyze conducting and semiconducting lines presented as distributed RC parameters. 5. To explain the principle of large capacitance driving. 6. To give and to explain the dynamics characteristics, and to estimate power dissipation in semiconductor integrated circuits. 7. To perform the synthesis of digital electronic circuits implementing the logical operations. 8. To perform DC, AC and transient analysis of electronic circuits using simulation tools.			
Lecturer / Teaching assistant	Prof. dr Nikša Tadić - professor, dr Milena Erceg –teaching assistant.			
Methodology	Lectures, exercises and laboratory exercises. Learning and homework. Consultations.			
Plan and program of work				
Preparing week	Preparation and registration of the semester			
I week lectures	Introduction: the types of substrates, fabrication technologies, fabrication techniques, integration scales, and semiconductor integrated circuit design methodologies			
I week exercises	Introduction to the integrated circuit design software tool			
II week lectures	MOSFET, BJT			
II week exercises	MOSFET as an amplifier			
III week lectures	CMOS inverter			
III week exercises	DC transfer characteristic and transient response of CMOS inverter			
IV week lectures	Bilateral CMOS switch			
IV week exercises	Transient response of bilateral CMOS switch			
V week lectures	Planar process			
V week exercises	Czochralski method of crystal growth video			
VI week lectures	Midterm			
VI week exercises	Midterm			
VII week lectures	Estimation of resistances, capacitances, and inductances			
VII week exercises	Common-source amplifier frequency response dependence on MOSFET’s dimensions			
VIII week lectures	Distributed RC parameters			
VIII week exercises	Delay time reduction in long semiconductor and conductor lines			
IX week lectures	Large capacitive loads driving in digital systems			
IX week exercises	Large capacitive loads driving in digital systems			
X week lectures	Dynamic characteristics			
X week exercises	DC analysis of two-stage CMOS operational amplifier			
XI week lectures	Power dissipation			
XI week exercises	AC analysis and transient response of two-stage CMOS operational amplifier			

XII week lectures	Digital CMOS circuits, I part
XII week exercises	Realization of combinational circuits using domino logic
XIII week lectures	Digital CMOS circuits, II part
XIII week exercises	CMOS D flip-flop
XIV week lectures	Analog CMOS circuits, I part
XIV week exercises	DC analysis of the second generation current conveyor
XV week lectures	Analog CMOS circuits, II part
XV week exercises	AC analysis and transient response of the second generation current conveyor
Student workload	Per week: 3L+1E+0.5Lab + 3 hours and 30 minutes of independent work, including consultations.

Per week	**Per semester**
6 credits x 40/30=8 hours and 0 minuts 3 sat(a) theoretical classes 0 sat(a) practical classes 1 excercises **4 hour(s) i 0 minuts** of independent work, including consultations	Classes and final exam: **8 hour(s) i 0 minuts x 16 =128 hour(s) i 0 minuts** Necessary preparation before the beginning of the semester (administration, registration, certification): **8 hour(s) i 0 minuts x 2 =16 hour(s) i 0 minuts** Total workload for the subject: **6 x 30=180 hour(s)** Additional work for exam preparation in the preparing exam period, including taking the remedial exam from 0 to 30 hours (remaining time from the first two items to the total load for the item) **36 hour(s) i 0 minuts** Workload structure: **128 hour(s) i 0 minuts (cources), 16 hour(s) i 0 minuts (preparation), 36 hour(s) i 0 minuts (additional work)**
Student obligations	Students are obligated to attend lectures and exercises.
Consultations	Consultations with Professor and Teaching Assistant, during the first 15 weeks of the semester.
Literature	Script: N. Tadić, VLSI Design
Examination methods	Midterm up to 50 points, and final exam up to 50 points.
Special remarks	
Comment	

Grade:	F	E	D	C	B	A
Number of points	less than 50 points	greater than or equal to 50 points and less than 60 points	greater than or equal to 60 points and less than 70 points	greater than or equal to 70 points and less than 80 points	greater than or equal to 80 points and less than 90 points	greater than or equal to 90 points